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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,875	09/29/2003	Mahesh J. Deshmane	42P17507	6817

8791 7590 04/20/2007

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EXAMINER	
SUGENT, JAMES F	
ART UNIT	**PAPER NUMBER**
2116	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/675,875	DESHMANE ET AL.	
	Examiner	Art Unit	
	James F. Sugent	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-7, 9-11,13-16,18,19,21,22,24,26 and 27* is/are rejected.

7)☒ Claim(s) *8,17,20,22 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is sent in response to Applicant's Communication received January 23, 2007 for application number 10/675,875 originally filed September 29, 2003. The Office hereby acknowledges receipt of the following and placed of record in file: amended claims 1-28 are presented for examination wherein claims 2, 3, 12, 23 and 25 are canceled.

Claim Objections

Claim 24 objected to because of the following informalities: claim 24, line 1 recites "The *computer system* of claim 22..." There is insufficient antecedent basis for this limitation in the claim. Change "The *computer system* of claim 22..." to read "The *apparatus* of claim 22..."

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 4-7, 9-11, 13-16, 18, 19, 21, 22, 24, 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (U.S. Patent No. 6,477,592 B1) (hereinafter referred to as Chen) in view of Namiki (U.S. Patent No. 4,704,642) (hereinafter referred to as Namiki).

As to claim 1, Chen discloses a computer system comprising: a bus (Figs. 2 and 5); and a chipset (22), coupled to the bus (as shown in Figs. 2 and 5), having: an input/output (I/O) buffer (44 and/or 46), coupled to the bus (as shown in Fig. 5), to transmit an output signal from the chipset via the bus (column 13, lines 4-38); and, control logic (slew control circuit 56) to detect the slew rate of a signal and to adjust the slew rate based upon the state of the signal (Chen discloses the control circuit 56 adjusts the slew rate of an outgoing signal based upon the slew rate that itself detects; column 13, lines 26-38 and column 11, line 65 thru column 12, line 13).

Although Chen teaches a slew control circuit to detect and adjust slew, Chen does not explicitly disclose a slew rate detection mechanism, coupled to the bus, to detect a slew rate of the output signal buffer and to generate a signal indicating a status of the slew rate; and, the control logic is coupled to the slew rate detection mechanism to transmit the signal indicating the slew rate.

Namiki teaches a noise reduction circuit comprising an output buffer (39), a slew rate detection circuit (47) and a slew control circuit (27B) (column 3, lines 30-46 and column 9, lines 14-30 and Fig. 8). Specifically, Namiki further teaches the output buffer (39) sending an output signal on a bus wherein slew rate detection circuit (47) detects the slew rate, sends a control signal to control circuit (27B) wherein the said control circuit adjusts the slew rate based upon the control signal (column 9, lines 14- 53). Namiki has the additional feature of overcoming any noise error during anytime of the transmission cycle (column 2, line 50 thru column 3, line 29).

It would have been obvious to one of ordinary skill of the art having the teachings of Chen and Namiki at the time the invention was made, to modify the chipset of Chen to include the slew detection circuit which produces a slew control signal as taught by Namiki. One of ordinary skill in the art would be motivated to make this combination of including a slew detection circuit which produces a slew control signal in view of the teachings of Chen, as doing so would give the added benefit of overcoming any noise error during anytime of the transmission cycle (as taught by Chen above).

As to claim 11, Chen discloses a computer system comprising: a main memory device (14 and Fig. 3); a memory bus coupled to the main memory device (as shown in Figs. 2 and 5); and a memory controller (22), coupled to the bus, having: an input/output (I/O) buffer (44 and/or 46), coupled to the bus, to transmit an output signal from the memory controller via the bus (column 13, lines 4-38); and, control logic (slew control circuit 56) to detect the slew rate of a signal and to adjust the slew rate based upon the state of the signal (Chen discloses the control circuit 56 adjusts the slew rate of an outgoing signal based upon the slew rate that itself detects; column 13, lines 26-38 and column 11, line 65 thru column 12, line 13).

Although Chen teaches a slew control circuit to detect and adjust slew, Chen does not explicitly disclose a slew rate detection mechanism, coupled to the bus, to detect a slew rate of the output signal buffer and to generate a signal indicating a status of the slew rate; and, the control logic is coupled to the slew rate detection mechanism to transmit the signal indicating the slew rate.

Namiki teaches a noise reduction circuit comprising an output buffer (39), a slew rate detection circuit (47) and a slew control circuit (27B) (column 3, lines 30-46 and column 9, lines 14-30 and Fig. 8). Specifically, Namiki further teaches the output buffer (39) sending an output signal on a bus wherein slew rate detection circuit (47) detects the slew rate, sends a control signal to control circuit (27B) wherein the said control circuit adjusts the slew rate based upon the control signal (column 9, lines 14- 53). Namiki has the additional feature of overcoming any noise error during anytime of the transmission cycle (column 2, line 50 thru column 3, line 29).

It would have been obvious to one of ordinary skill of the art having the teachings of Chen and Namiki at the time the invention was made, to modify the chipset of Chen to include the slew detection circuit which produces a slew control signal as taught by Namiki. One of ordinary skill in the art would be motivated to make this combination of including a slew detection circuit which produces a slew control signal in view of the teachings of Chen, as doing so would give the added benefit of overcoming any noise error during anytime of the transmission cycle (as taught by Chen above).

As to claim 18, Chen discloses a method comprising: transmitting a signal from an input/output (I/O) buffer (44 and/or 46) within a chipset (22) over a bus (column 13, lines 4-38 and Figs. 2 and 5); generating a signal (via control circuit 56) indicating the status of the slew

rate; and, adjusting the slew rate at control logic (56) within the chipset based upon the signal (Chen discloses the control circuit 56 adjusts the slew rate of an outgoing signal based upon the slew rate that itself detects; column 13, lines 26-38 and column 11, line 65 thru column 12, line 13).

Although Chen teaches a slew control circuit to detect and adjust slew, Chen does not explicitly disclose receiving the signal at a slew rate detection mechanism within the chipset via the bus.

Namiki teaches a noise reduction circuit comprising an output buffer (39), a slew rate detection circuit (47) and a slew control circuit (27B) (column 3, lines 30-46 and column 9, lines 14-30 and Fig. 8). Specifically, Namiki further teaches the output buffer (39) sending an output signal on a bus wherein slew rate detection circuit (47) detects the slew rate, sends a control signal to control circuit (27B) wherein the said control circuit adjusts the slew rate based upon the control signal (column 9, lines 14- 53). Namiki has the additional feature of overcoming any noise error during anytime of the transmission cycle (column 2, line 50 thru column 3, line 29).

It would have been obvious to one of ordinary skill of the art having the teachings of Chen and Namiki at the time the invention was made, to modify the chipset of Chen to include the slew detection circuit which produces a slew control signal as taught by Namiki. One of ordinary skill in the art would be motivated to make this combination of including a slew detection circuit which produces a slew control signal in view of the teachings of Chen, as doing so would give the added benefit of overcoming any noise error during anytime of the transmission cycle (as taught by Chen above).

As to claim 22, Chen discloses an apparatus comprising: an input/output (I/O) buffer (44 and/or 46) to transmit an output signal (column 13, lines 4-38 and Figs. 2 and 5); a control circuit (56) to detect the slew rate of the output signal transmitted from the I/O buffer over a bus and to generate a signal to indicate the status of the slew rate (Chen discloses the control circuit 56 adjusts the slew rate of an outgoing signal based upon the slew rate that itself detects; column 13, lines 26-38 and column 11, line 65 thru column 12, line 13).

Although Chen teaches a slew control circuit to detect and adjust slew, Chen does not explicitly disclose a slew rate detection mechanism coupled to receive the output signal from the I/O buffer via a bus.

Namiki teaches a noise reduction circuit comprising an output buffer (39), a slew rate detection circuit (47) and a slew control circuit (27B) (column 3, lines 30-46 and column 9, lines 14-30 and Fig. 8). Specifically, Namiki further teaches the output buffer (39) sending an output signal on a bus wherein slew rate detection circuit (47) detects the slew rate, sends a control signal to control circuit (27B) wherein the said control circuit adjusts the slew rate based upon the control signal (column 9, lines 14- 53). Namiki has the additional feature of overcoming any noise error during anytime of the transmission cycle (column 2, line 50 thru column 3, line 29).

It would have been obvious to one of ordinary skill of the art having the teachings of Chen and Namiki at the time the invention was made, to modify the chipset of Chen to include the slew detection circuit which produces a slew control signal as taught by Namiki. One of ordinary skill in the art would be motivated to make this combination of including a slew detection circuit which produces a slew control signal in view of the teachings of Chen, as doing

so would give the added benefit of overcoming any noise error during anytime of the transmission cycle (as taught by Chen above).

As to claims 4 and 13, Chen in combination with Namiki taught the computer systems in claims 1 and 11, as shown above. Chen further discloses the computer system wherein the control logic reduces the slew rate if the signal received from the slew rate detection mechanism indicates that the slew rate is too fast (Chen discloses increasing or decreasing slew transition dependent on the measured slew rate; column 11, line 65 thru column 12, line 21).

As to claims 5 and 14, Chen in combination with Namiki taught the computer systems in claims 1 and 11, as shown above. Chen further discloses the computer system wherein the control logic increases the slew rate if the signal received from the slew rate detection mechanism indicates that the slew rate is too slow (Chen discloses increasing or decreasing slew transition dependent on the measured slew rate; column 11, line 65 thru column 12, line 21).

As to claims 6, 15, and 26, Chen in combination with Namiki taught the computer systems and apparatus in claims 1, 11 and 22, as shown above. Chen further discloses the computer system and apparatus wherein the slew rate detection mechanism includes a capacitor, coupled to the bus, to integrate the received signal current (column 17, lines 32-54).

As to claims 7, 16, 19 and 27, Chen in combination with Namiki taught the computer systems, apparatus and method in claims 6, 15, 18, and 26, as shown above. Namiki further discloses the computer system, apparatus and method wherein the slew rate detection mechanism further includes: a reference current generator (57) to generate a reference current; and, a comparator (56) to compare the received signal current to the reference current (column 12, lines 12-31).

As to claims 9 and 21, Chen in combination with Namiki taught the computer system and method in claims 6 and 18, as shown above. Namiki further discloses the computer system, apparatus and method wherein the comparator is an operational amplifier (column 9, lines 14-30 and column 12, lines 12-31).

As to claim 10, Chen in combination with Namiki taught the computer system in claim 1, as shown above. Chen further discloses the computer system wherein the bus is a high-speed bus (column 2, lines 2-4 and column 11, lines 50-54 and column 15, lines 46-55).

As to claim 24, Chen in combination with Namiki taught the computer system in claim 22, as shown above. Namiki further discloses the computer system further comprising control logic, coupled to the I/O buffer and the slew rate detection mechanism, to receive the signal and modify the slew rate based upon the signal (column 9, lines 14- 53).

Allowable Subject Matter

Claims 8, 17, 20 and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments, see Arguments/Remarks, filed September 23, 2007, with respect to the rejection(s) of claim(s) 1, 11, 18 and 22 under 35 USC § 102 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further

consideration, a new ground(s) of rejection is made in view of Chen in view of Namiki (both as cited above).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Schultz (US 6388486 B1) teaches a dynamic slew rate correction system for output data.

Hunley (US 5877634 A) teaches a method and apparatus for a circuit physically realizing a CMOS buffer with a controlled slew rate at the output and using no additional standby power to achieve the slew rate control with a feedback path from the output

Zumkehr et al. (US 6617895 B2) teaches a device and method for calibrating a slew rate on output data.

Jenkins (US 6184708 B1) teaches a system on a PLD with IOBs wherein each output buffer is coupled to an associated adjustable slew rate control circuit and to an adjustable delay line.

Williams et al. (US 6237107 B1) teaches a circuit comprising an output circuit, an adjustment circuit and a detect circuit wherein the slew rate adjustor circuit may be configured to present the control signals to adjust slew.

Donnelly et al. (US 5959481 A) teaches a bus driver circuit having slew rate control that measures the slew rate on output data, creates a control signal and uses said control signal to adjust the slew rate.

Lee et al. (US 6614285 B2) teaches a system that controls power in a device to compensate for a measured slew rate.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The Examiner can normally be reached on 8AM - 4PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call (800) 786-9199 (IN USA OR CANADA) or (571) 272-1000.

James F. Sugent
Patent Examiner, Art Unit 2116
April 11, 2007

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
4/16/07